**HO CHI MINH UNIVERSITY OF TECHNOLOGY**

**OFFICE FOR INTERNATIONAL STUDY PROGRAMS - OISP**

**Logic Design with HDL**

EXPERIMENT

**Combinational Logic Circuit**

**Group information:**

| Class : Logic Design with HDL (Lab)  Group : 2 | Lecturer’s comment |
| --- | --- |
| Full name:   1. Nguyễn Văn Bình : 2153223 2. Lê Minh Quý : 2153758 3. Trần Hải Đăng : 2153297 4. Phạm Đức Trung : 2153928 |  |

**1 Introduction**

**1.1 Aims**

• Practice in designing combinational logic circuits using Verilog HDL continuous assignment.

• Practice in designing combinational logic circuits using Verilog HDL blocking assignment in behavioral model.

**1.2 Preparation**

• Read the laboratory materials before class.

• Review chapter 4-5 about Dataflow model and continuous assignment, Behavioral model.

**1.3 Report Requirements**

• Lab exercises will be reviewed directly in class.

• Write report (with circuit/simulation screenshots inserted) in pdf.

• Must have group ID, group member’s names and student IDs in the report.

• Compress the report with code files (only .v files) in only one .zip file, name the .zip the group ID (for example: Nhom 1.zip).

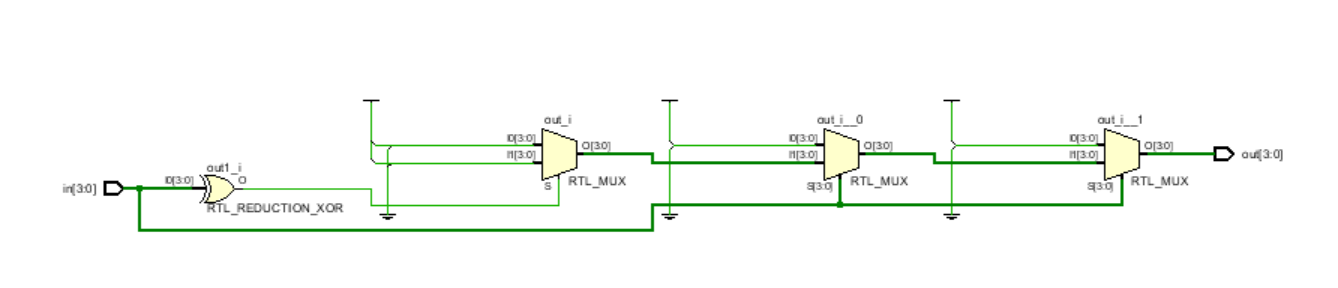
• Submit on BK-elearning by deadline.

**2 Exercises**

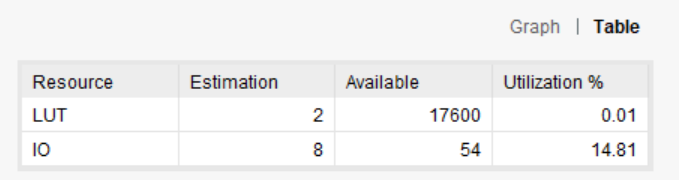
**2.1 Exercises 1**

- Name of source files : ex1.v, ex1\_tb.v

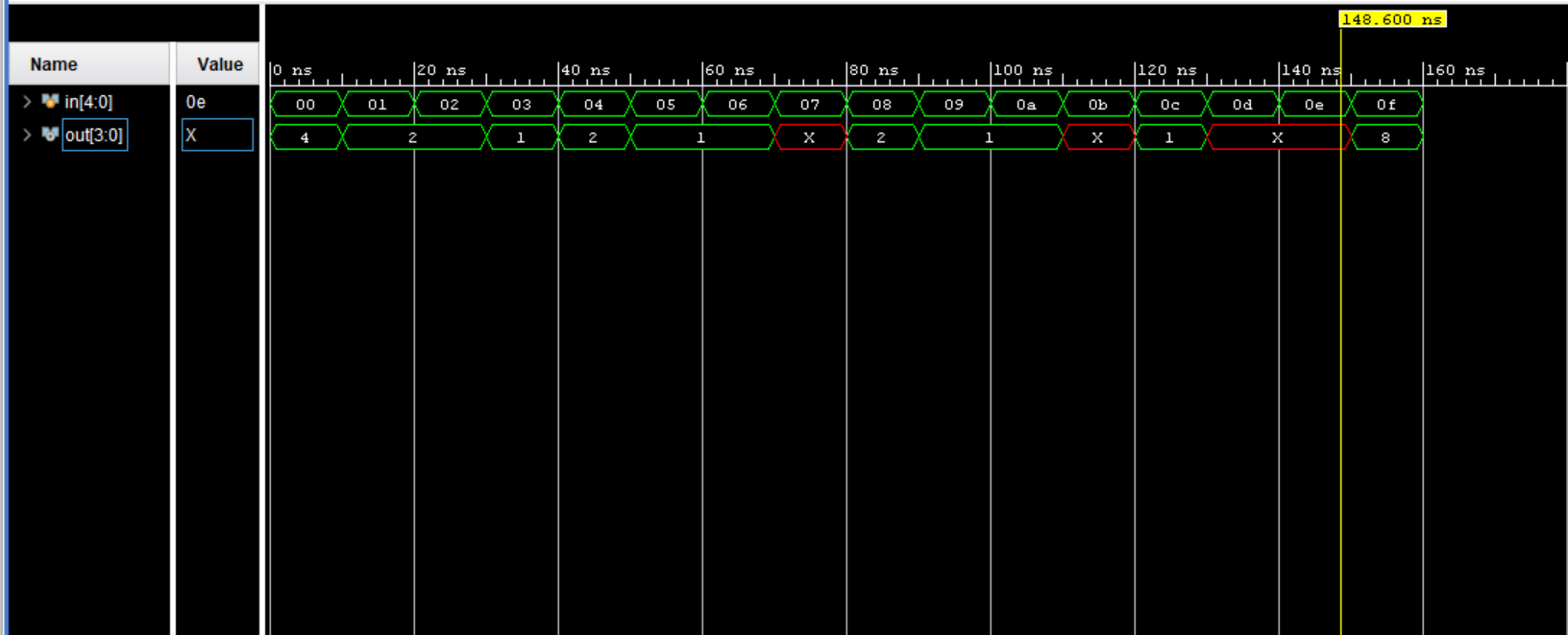
- RTL Schematic



-Resource Utilization



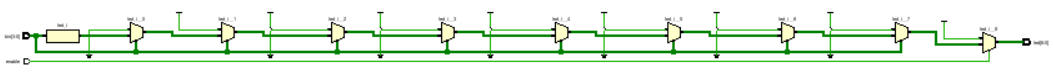
- Waveform



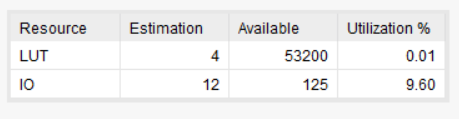
**2.2 Exercises 2**

- Source files : ex2.v, ex2\_tb.v

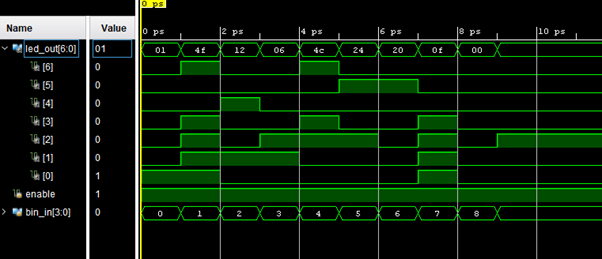
- RTL Schematic:



- Utilization



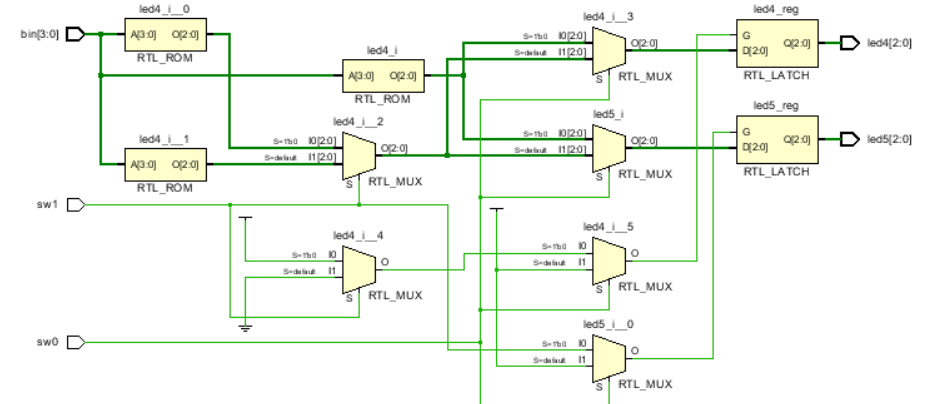
- Waveform



**2.3 Exercises 3**

-Source files : ex3.v, ex3\_tb.v

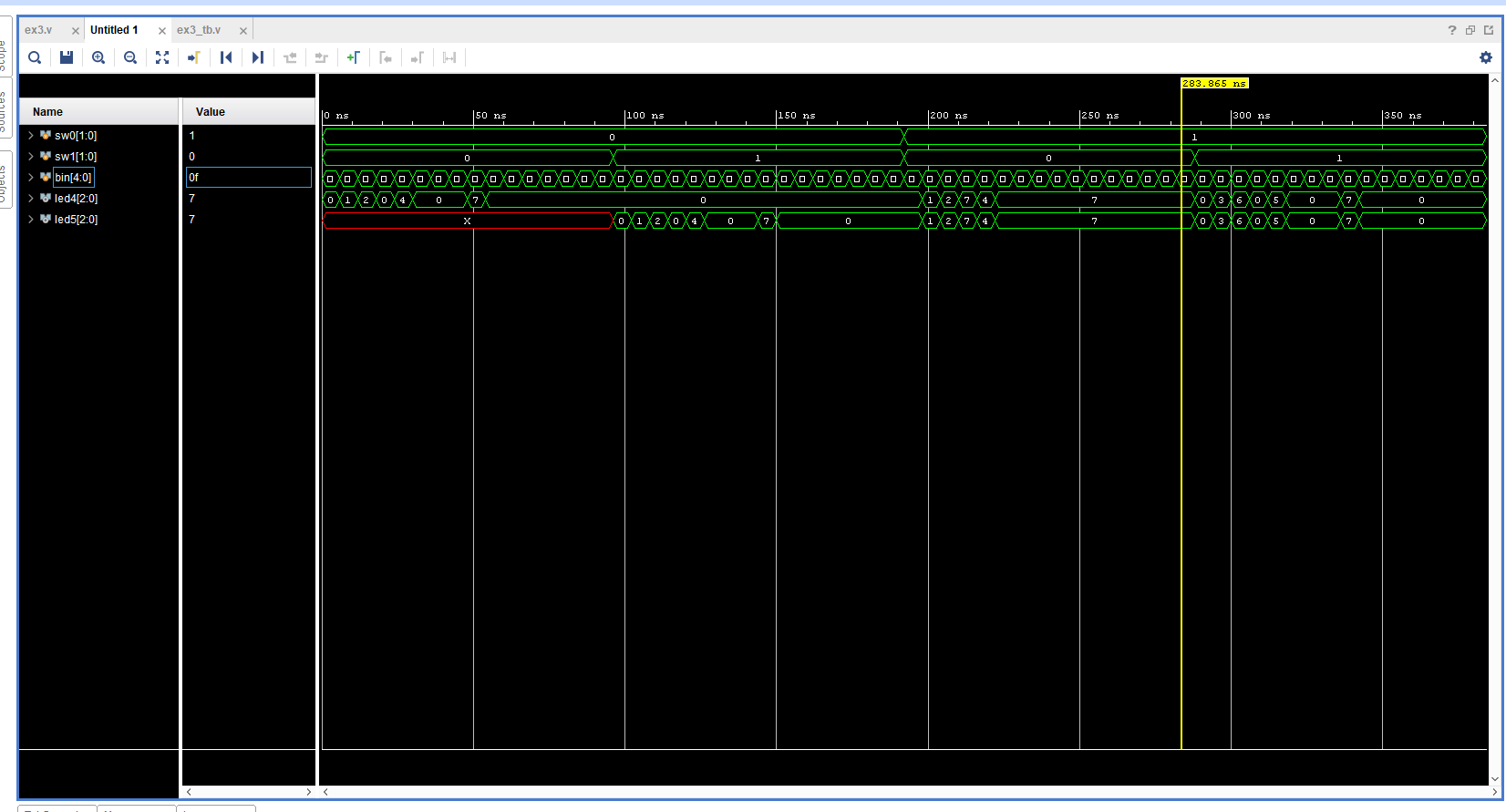
-RTL Schematic :



-Utilization



-Waveform



**End.**